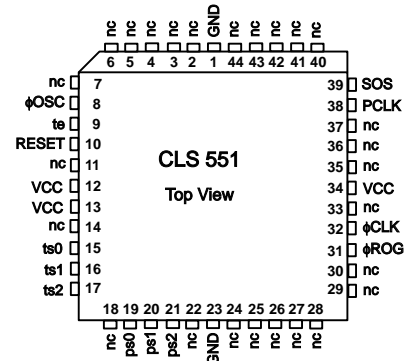


CLS 551

ccd linescan
controller

Key Features:

- CCD Linescan controller
- Designed for Sony ILX 551
- All clock signals included.
- Start of frame output.
- Selectable exposure time.



Overview:

The CLS 551 is an easy to use, complete ccd linescan controller, designed for the SONY ILX 551 linescan sensor.

For operation the CLS 551 requires power +5 V only, and a 10 MHz TTL or CMOS clock input signal. Additional logic is not required.

To provide more flexibility, the CLS 551 has an interface to control exposure time and pixel clock. All inputs are connected to internal pull up resistors, so they can left unconnected if not required.

Interface:

The CLS 551 linescan controller includes all CCD-timing signals including pixel clock and exposure control.

The digital interface provides user selectable pixel clock and exposure time. An output for pixel clock and start of frame facilitates the operation with an additional frame grabber.

With an additional oscilloscope and a Sony IILX 551 CCD-sensor the CLS 551 converts to a complete very low cost CCD-linescan camera with display. (See the application on the last page).

Absolute Maximum Ratings

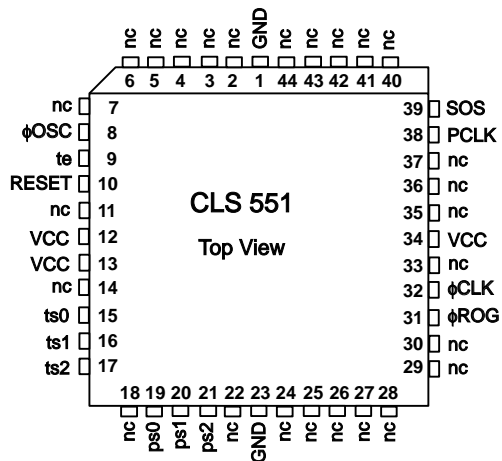
VCC Supply voltage	- 0.5 V to + 6 V
Input voltage applied	- 0.5 to Vcc + 0.5 V
Digital output current	0 to 5 mA
Storage temperature	- 20 to 150 °C
Operating temperature	0 to 50 °C

DC Characteristics

Output low voltage (8 mA)	0.4V
Output high voltage (-4 mA)	2.4V
Input pullup current	-0.15 mA
Input low Voltage (max)	0.8 V
Input high voltage (min)	2.0V
Power requirements:	+5V 200mA

khs instruments

Pin Configuration



44-Pin PLCC Pinout Diagram

User Interface

Connections:

Signal	Pin	Pin	Signal
SOS	39	10	Reset
PCLK	38	8	ϕ OSC
ts2	17	21	ps2
ts1	16	20	ps1
ts0	15	20	ps0
te	9		

All inputs: 50 K pull up to VCC.

Pinout description:

Pin Name	Pin Type	Pin Description
SOS	OUT	Start of scan output, low active.
PCLK	OUT	Pixelclock output, low active.
ts0..ts1	IN	Exposure control.
te	IN	Exposure control external.
ps0..ps1	IN	Pixelclock control.
ϕ OSC	IN	Oscillator input
Reset	IN	CCD asynchron reset low active
nc	NC	Do not connect!

CCD Interface

Connections:

Signal	Pin
ϕ CLK	32
ϕ ROG	31

Pinout description:

Pin Name	Pin Type	Pin Description
ϕ CLK	OUT	Clock pulse
ϕ ROG	OUT	Readout gate pulse

Power

Connections:

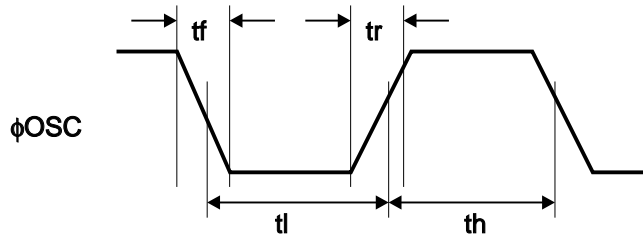
Signal	Pin
GND	1
GND	23
VCC	12
VCC	13
VCC	34

Pinout description:

Pin Name	Pin Type	Pin Description
GND	Power	Power Ground.
VCC	Power	Power + 5 V.

CLS 551

φOsc Timing



Item	Symbol	Min.	Typ.	Max.	Unit
φOSC pulse Duty ^{**}	-	-	50	-	%
φOSC pulse rise / fall time	tr, tf	0	10	20	ns
φOSC frequency	-	-	10	10	MHz

^{**}100 x th / (tl + th)

Exposure timer control

Note: For timing details see t16, page 4

ts2	ts1	ts0	exposure time
1	1	1	2088 τ
1	1	0	4096 τ
1	0	1	8192 τ
1	0	0	16384 τ
0	1	1	32768 τ
0	1	0	65536 τ
0	0	0	extern

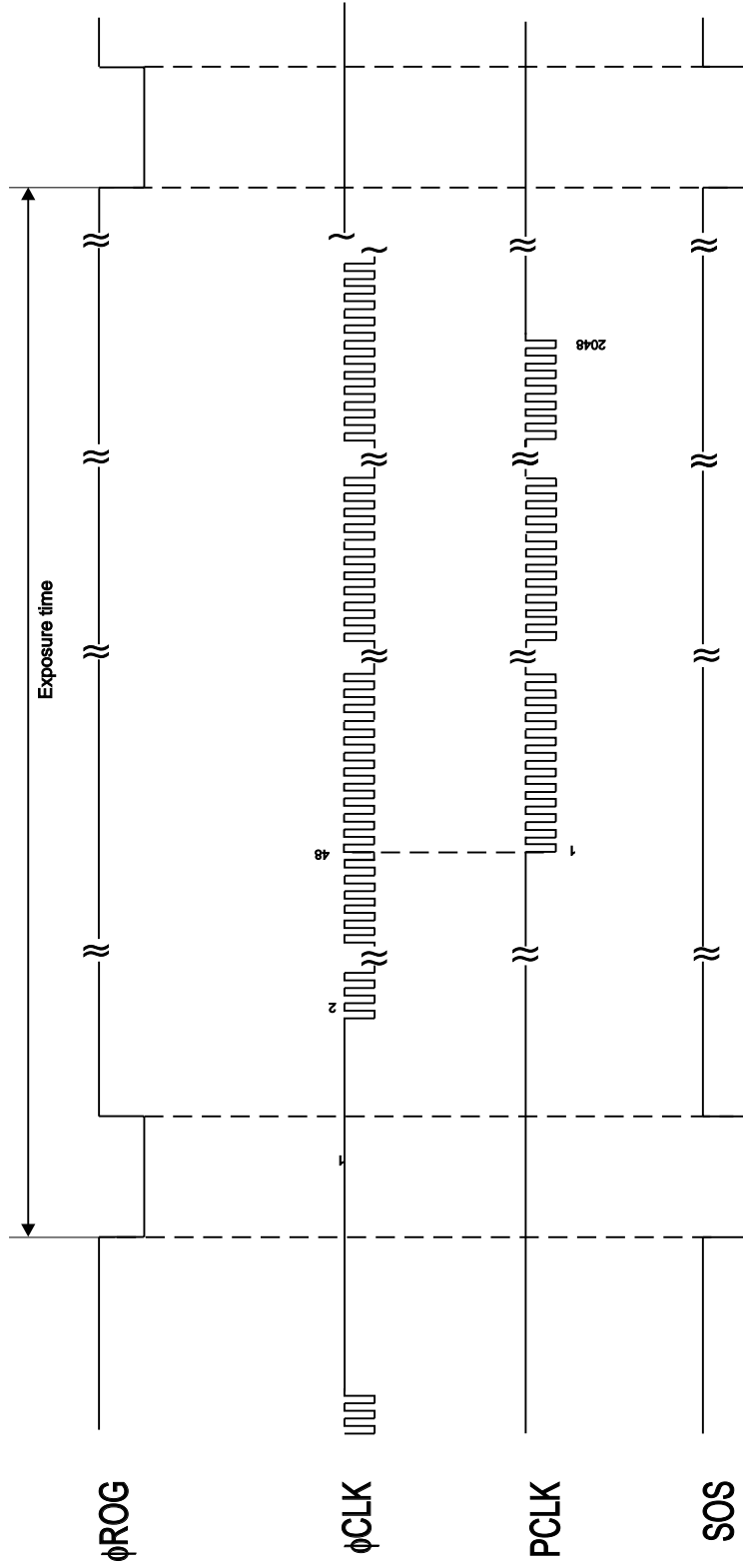
Note) τ is the period of φCLK (τ = 200 ns at 5 MHz).

Pixelclock control

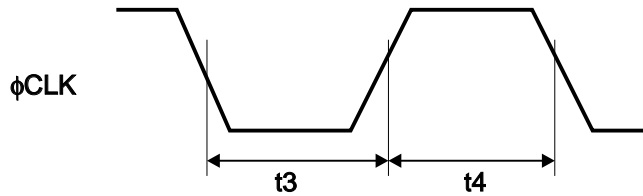
ps2	ps1	ps0	φCLK	(at 10 MHz φCLK)
1	1	1	1/2 φOsc	(5 MHz)
1	1	0	1/4 φOsc	(2.5 MHz)
1	0	1	1/8 φOsc	(1.25 MHz)
1	0	0	1/16 φOsc	(625 KHz)

CLS 551

Clock Timing Diagram



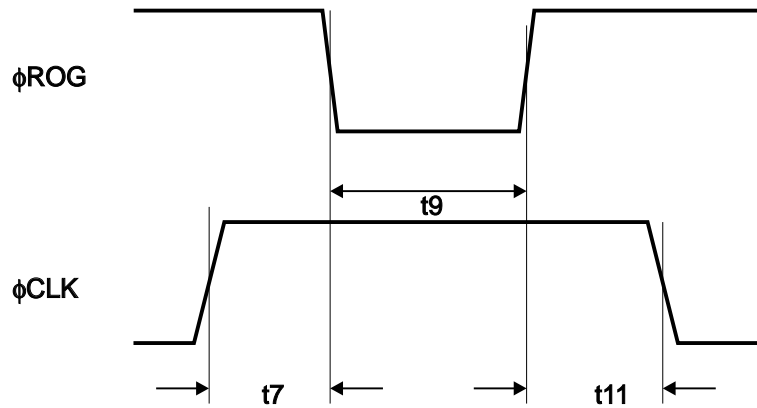
φCLK Timing



Item	Symbol	Min.	Typ.	Max.	Unit
φCLK pulse Duty ^{**1}	-	-	50	-	%

^{**1} $100 \times t4 / (t3 + t4)$

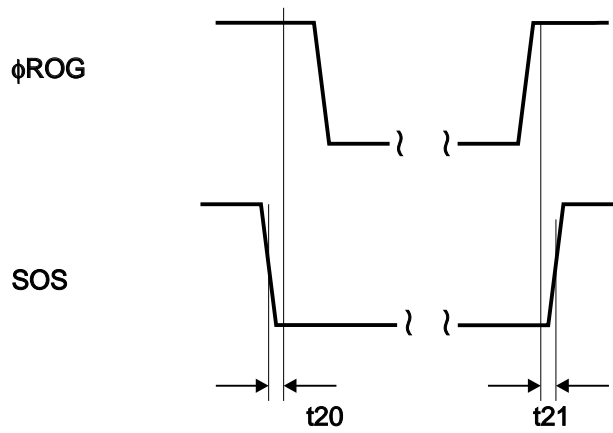
φROG, φCLK Timing



Item	Symbol	Min.	Typ.	Max.	Unit
φROG φCLK pulse timing 1	t7	-	10 τ	-	ns
φROG φCLK pulse timing 2	t11	-	6 τ	-	ns
φROG pulse period	t9	-	8 τ	-	ns

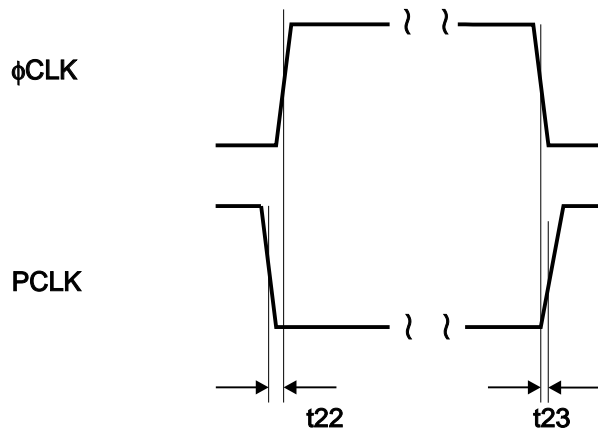
Note) τ is the period of φCLK.

ϕ ROG, SOS Timing



Item	Symbol	Min.	Typ.	Max.	Unit
ϕ ROG SOS pulse timing 1	t20	-10	0	10	ns
ϕ ROG SOS pulse timing 2	t21	-10	0	10	ns

ϕ CLK, PCLK Timing

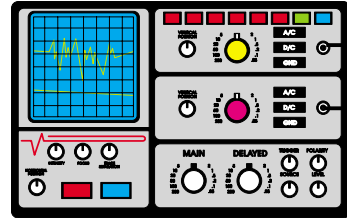


Item	Symbol	Min.	Typ.	Max.	Unit
ϕ CLK PCLK pulse timing 1	t22	-10	0	10	ns
ϕ CLK PCLK pulse timing 2	t23	-10	0	10	ns

Application

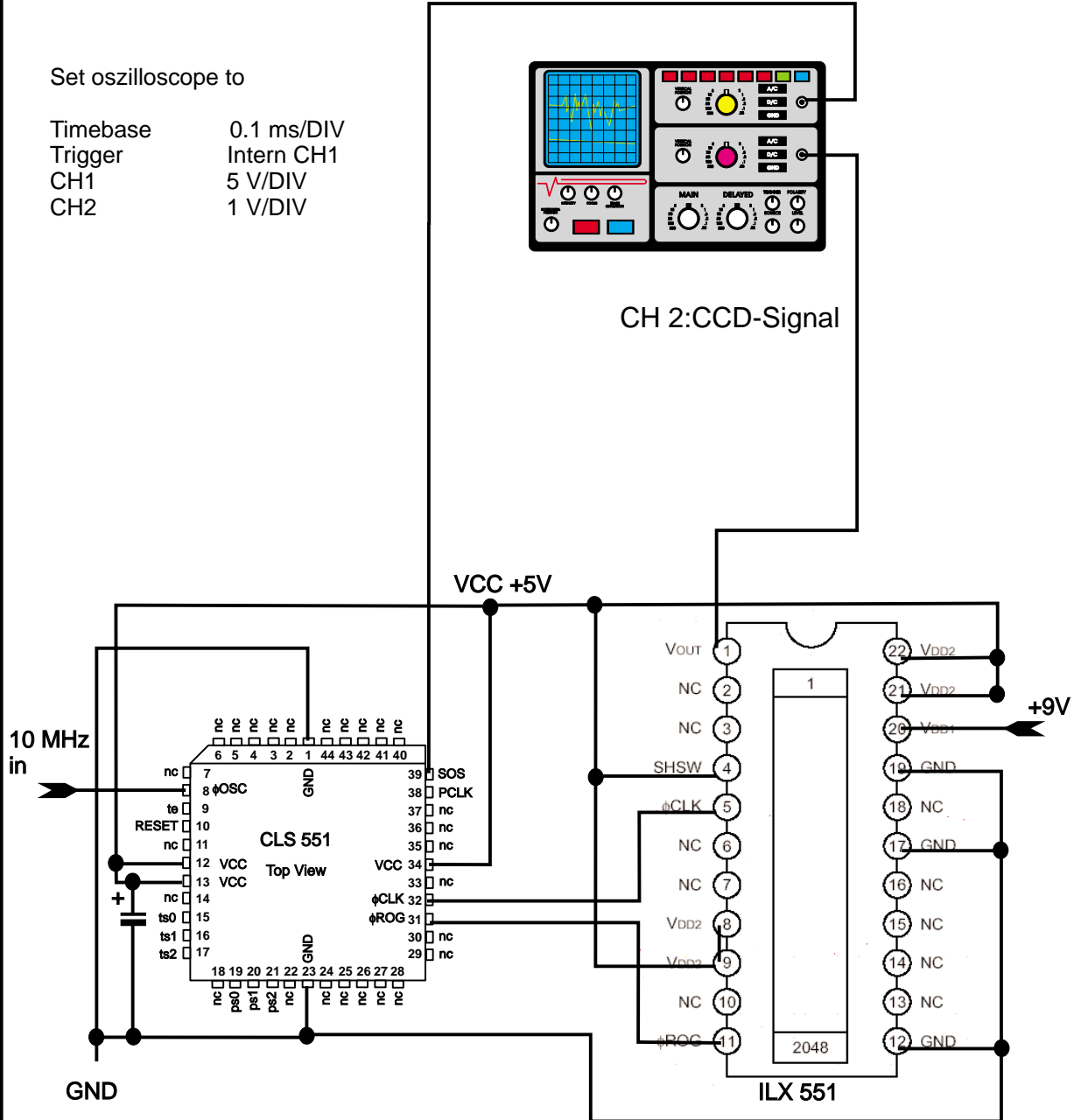
Set oszilloscope to

Timebase 0.1 ms/DIV
 Trigger Intern CH1
 CH1 5 V/DIV
 CH2 1 V/DIV



CH 1: Trigger

CH 2: CCD-Signal



See SONY ILX 551 datasheet for more details.

CLS 551

Fig. 1 Test circuit