

khs

instruments

analog::blocks

***standard specification
modular Analog Test and
Development Platform***

Rev. 1.0

Contents

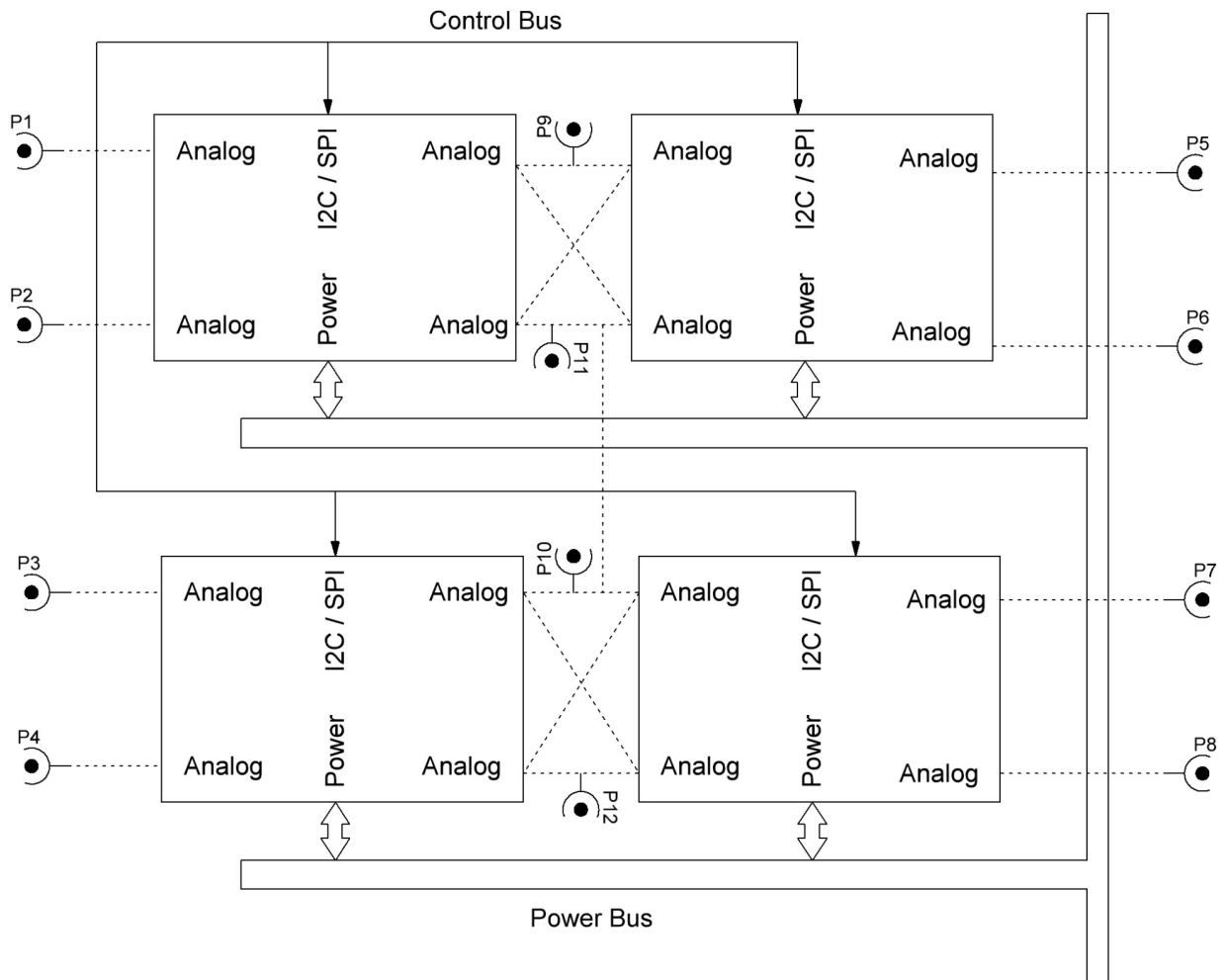
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1 Scope

analog::blocks is a modular hardware standard for analog and mixed-signal development. It provides common power and digital control infrastructure while keeping analog signal routing as an explicit part of the system architecture. Module size is not fixed; compatibility is defined by the interface and the module grid.

2 Basic Architecture

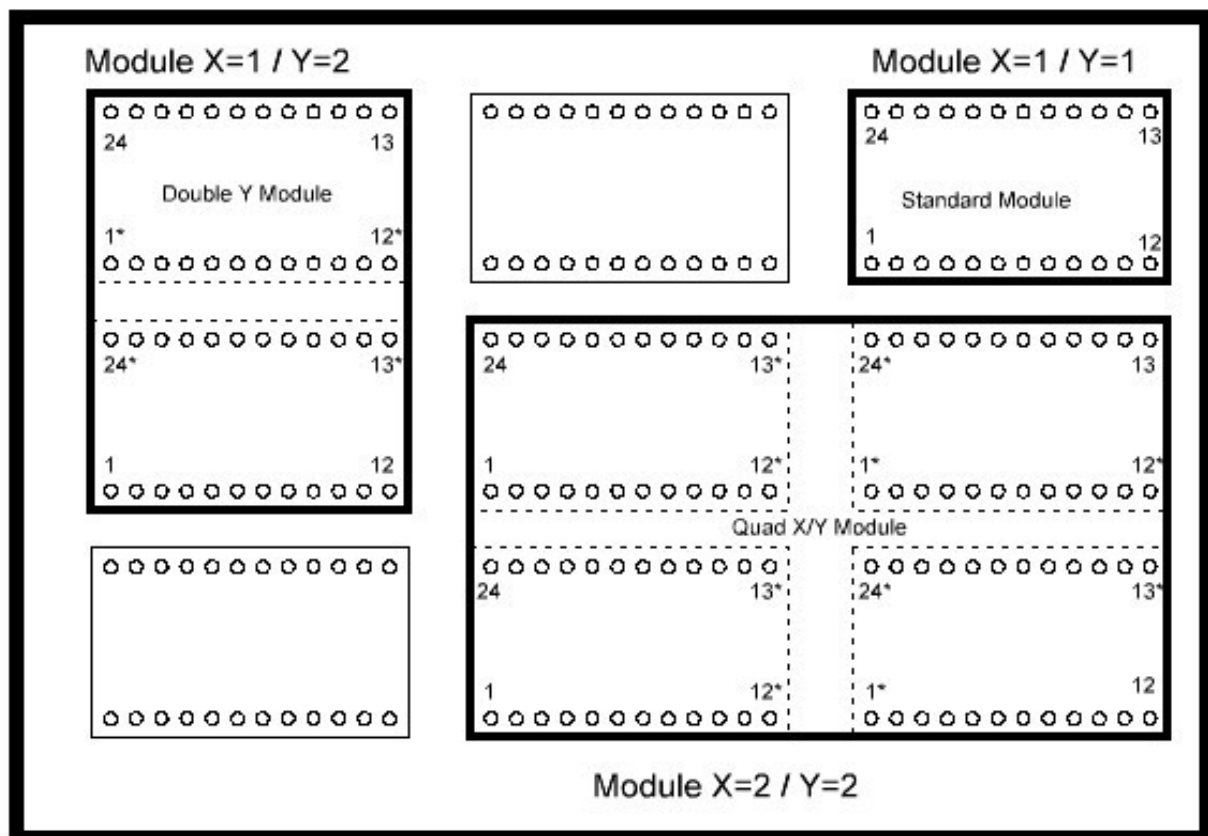
Power and control signals are distributed by common buses. Analog signals are routed separately between module positions and external connections.



3 Module Size Concept

A standard module occupies one module position. Larger modules may occupy multiple positions in X and/or Y. Additional connector positions covered by a larger module are optional and may be populated as required by the module.

Ground Plane



* optional pins

4 Mechanical Interface

The mechanical layout is based on the following fixed grid dimensions:

Parameter	Value
Basic PCB / ground-plane grid	100 mil (2.54 mm)
Connector pin pitch	100 mil (2.54 mm)
Connector row spacing	600 mil (15.24 mm)
Module pitch Y	900 mil (22.86 mm)
Module pitch X	1800 mil (45.72 mm)

Pin 1 follows the conventional DIL orientation and is identified by a chamfered corner of the module PCB.

The chamfer is a visual orientation aid and does not mechanically prevent reverse insertion. All GND pins of a compatible module shall be electrically connected together on the module. This provides multiple parallel ground connections between module and base board and distributes return current across the available contacts.

5 Module Interface and Pin Assignment

The module interface consists of 24 contacts. The four corner contacts are the principal analog signal connections. The signal names IN and OUT describe their usual purpose; an individual module may use these analog contacts in the opposite direction.

Pinout

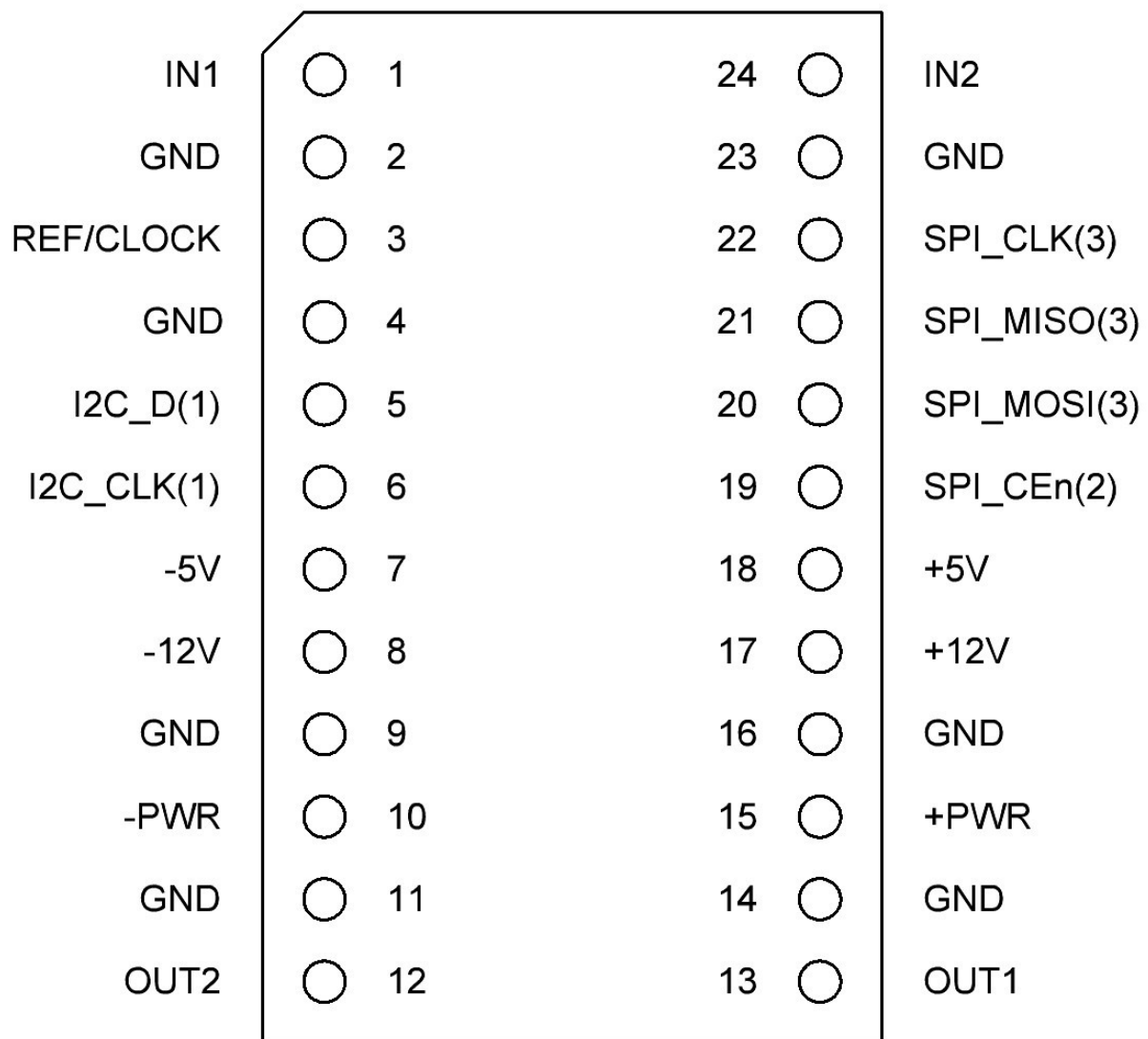


Figure 3:

24-pin analog::blocks module interface, top view.

(1) I2C lines may be used as general-purpose lines when I2C is not used.

(2) SPI-CE is active LOW.

(3) SPI lines may be used as general-purpose module lines when selected by SPI-CE.

6 Ground and PCB Routing

Ground is an integral part of the analog::blocks interconnect structure. Most signal and power traces are surrounded by ground. Standard signal and power traces are nominally 24 mil (0.61 mm) wide with 5 mil (0.127 mm) spacing to surrounding ground. Dedicated analog traces are nominally 50 mil (1.27 mm) wide and are also surrounded by ground.

A 50 ohm characteristic impedance is a property of specially designed transmission paths and shall not be inferred from trace width alone.

7 Power Interface and Protection

Rail	Nominal / limit	Requirement
+5 V	+5 V,	Used by system functions including optional EEPROMs and electrical isolation; approx. 5.6 V Zener protection on base board.
-5 V	-5 V	Approx. 5.6 V Zener protection on base board.
+12 V	+12 V	nominal Modules shall tolerate up to +15 V; approx. 16 V Zener protection on base board.
-12 V	-12 V	nominal Modules shall tolerate down to -15 V; approx. 16 V Zener protection on base board.
+PWR / -PWR	Up to +-30V relative to GND	Auxiliary rails; reverse-polarity protection on the base board protects connected modules against an incorrectly connected external supply.
Current	1 A continuous	Maximum continuous current per standard power rail.

A module that generates or drives a supply rail shall comply with the voltage, polarity and current limits defined for that rail.

8 Digital Interface

The standardized digital interface uses 3.3 V logic. I²C uses open-drain signaling with system pull-ups to 3.3 V. SPI uses 3.3 V CMOS-compatible signaling. REF/CLOCK is user-definable and is not restricted to the standardized 3.3 V digital bus unless used as a digital signal by the application.

Signal	Direction	Electrical / protocol
I ² C Data	I/O	Open-drain, 3.3 V pull-up
I ² C Clock	I	Open-drain, 3.3 V pull-up
SPI-CE	I	3.3 V CMOS, active LOW
SPI-MOSI	I	3.3 V CMOS
SPI-MISO	O	3.3 V CMOS; unselected modules shall not drive the line
SPI-Clock	I	3.3 V CMOS

I²C clock frequency: 100 kHz. SPI initially defines a low-speed compatibility mode. Higher rates may be supported by individual implementations.

9 Compatibility Requirements

A compatible module shall use the defined pin assignment and mechanical grid. Unused interface pins shall remain electrically unconnected.

Different interface signals and power rails shall not be interconnected unless explicitly permitted by this standard. GND pins are the exception and shall all be connected together on the module.

A module shall not drive a shared signal or power rail outside its specified voltage, polarity or current limits. This applies in particular to modules that generate supply voltages.

10 Standard Versioning

The standard uses a Major.Minor version number. Implementations with the same major version shall remain compatible. Minor revisions may add definitions or capabilities but shall not break compatibility with earlier revisions of the same major version.

History:		
Revision	date yymmdd	Changes
1.0	26/09/15	Initial.